Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **IN1**
2. **IN2**
3. **IN3**
4. **IN4**
5. **IN5**
6. **IN6**
7. **IN7**
8. **GND**
9. **COM**
10. **OUT10**
11. **OUT11**
12. **OUT12**
13. **OUT13**
14. **OUT14**
15. **OUT15**
16. **OUT16**

**.053”**

**.098”**

**1**

**2**

**3**

**4**

**5**

**6**

**7**

**16**

**15**

**14**

**13**

**12**

**11**

**10**

**8 9**

**MASK**

**REF**

**2003C**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004” min.**

**Backside Potential:**

**Mask Ref: 2003C**

**APPROVED BY: DK DIE SIZE .053” X .098” DATE: 10/4/22**

**MFG: TEXAS INSTRUMENTS THICKNESS .010” P/N: UNL2003**

**DG 10.1.2**

#### Rev B, 7/19/02